Efficient Utilization of Shared Buffer Memory
and Method for Operating the Same

ABSTRACT OF THE DISCLOSURE

5   Broadly speaking, an apparatus for efficiently utilizing a shared packet buffer memory in a switch and a method for operating the same is provided. More specifically, the apparatus includes a memory having a number of buffers configured to be operated in a ratcheted manner. The ratcheted manner in which the memory is operated causes each incoming data stream to be distributed across the number of buffers. Each stored data

10   stream can also be retrieved from the number of buffers for output from the memory in a similar ratcheted manner. The memory uses a rotating selector to control the ratcheted manner of operation. Also, the memory is capable of simultaneously servicing each of a number of inputs and a number of outputs to which the memory is connected.